

WHAT IS CLAIMED IS:

1                   1. An MPEG on-screen display coder comprising:  
2                   an on-screen display turn on device arranged to  
3 provide an output when an on-screen display is to be turned  
4 on; and,  
5                   an MPEG encoder arranged to encode frames with the  
6 on-screen display in response to the output of the on-screen  
7 display turn on device.

2. The MPEG on-screen display coder of claim 1  
wherein the MPEG encoder replaces original video frames with  
the encoded frames, and wherein the frames encoded with the  
on-screen display have a time base which is independent of  
the original video frames.

3. The MPEG on-screen display coder of claim 2  
wherein the on-screen display is overlaid on a solid color  
background.

1           4. The MPEG on-screen display coder of claim 2  
2 wherein the MPEG encoder is arranged to calculate a video  
3 hold off time dependent upon a number of frames in a decoder  
4 buffer of a digital television and to use the video hold off  
5 time so as to prevent overflow of the decoder buffer.

1           5. The MPEG on-screen display coder of claim 4  
2 wherein the MPEG encoder supplies the video hold off time to  
3 the on-screen display turn on device, and wherein the on-  
4 screen display turn on device permits the frames encoded  
5 with the on-screen display to be supplied to the digital  
6 television when the video hold off time expires.

1           6. The MPEG on-screen display coder of claim 1  
2 wherein the MPEG encoder replaces original video frames with  
3 the encoded frames, and wherein the frames encoded with the  
4 on-screen display have a time base which is slaved to the  
5 original video frames.

1           7. The MPEG on-screen display coder of claim 6  
2 wherein the on-screen display is overlaid on a solid color  
3 background.

1           8. The MPEG on-screen display coder of claim 6  
2 wherein the MPEG encoder is arranged to supply first and  
3 second I frame markers to the on-screen display turn on  
4 device, wherein the on-screen display turn on device causes  
5 the frames encoded with the on-screen display to be supplied  
6 to a digital television in response to the first I frame  
7 marker, and wherein the on-screen display turn on device  
8 causes the original video frames to be supplied to the  
9 digital television in response to the second I frame marker.

093307030904050607080910  
1           9. The MPEG on-screen display coder of claim 6  
2 wherein the MPEG encoder is arranged to supply a video I  
3 frame marker and an on-screen display I frame marker to the  
4 on-screen display turn on device, wherein the on-screen  
5 display turn on device causes the frames encoded with the  
6 on-screen display to be supplied to a digital television in  
7 response to the on-screen display I frame marker, and  
8 wherein the on-screen display turn on device causes the  
9 original video frames to be supplied to the digital  
10 television in response to the video I frame marker.

10. The MPEG on-screen display coder of claim 9 wherein the MPEG encoder signals the on-screen display I frame marker when the MPEG encoder generates an encoded I frame, and wherein the MPEG encoder signals the video I frame marker when an original I frame is received.

11. The MPEG on-screen display coder of claim 1 wherein the on-screen display is overlaid on video.

12. The MPEG on-screen display coder of claim 11 wherein the MPEG encoder is arranged to pass unchanged I frames.

13. The MPEG on-screen display coder of claim 12 wherein the MPEG encoder is arranged to encode a first P frame by predicting the first P frame from a preceding I frame with residuals in the predicted first P frame containing the on-screen display and with motion vectors set equal to zero, and wherein the MPEG encoder is arranged to encode subsequent P frames based upon the predicted first P frame with residuals and motion vectors set equal to zero.

1           14. The MPEG on-screen display coder of claim 13  
2 wherein the MPEG encoder is arranged to supply first and  
3 second I frame markers to the on-screen display turn on  
4 device, wherein the on-screen display turn on device causes  
5 the frames encoded with the on-screen display to be supplied  
6 to a digital television in response to the first I frame  
7 marker, and wherein the on-screen display turn on device  
8 causes original video frames to be supplied to the digital  
9 television in response to the second I frame marker.

10           15. The MPEG on-screen display coder of claim 14  
11 wherein the MPEG encoder signals the first and second I  
12 frame markers when corresponding original I frames are  
13 received.

14           16. The MPEG on-screen display coder of claim 11  
15 wherein the MPEG encoder is arranged to encode I frames with  
16 the on-screen display.

17           17. The MPEG on-screen display coder of claim 16  
18 wherein the MPEG encoder is arranged to encode subsequent P  
19 frames by prediction based upon the encoded I frames with  
20 residuals and motion vectors set equal to zero.

1           18. The MPEG on-screen display coder of claim 17  
2 wherein the MPEG encoder is arranged to supply first and  
3 second I frame markers to the on-screen display turn on  
4 device, wherein the on-screen display turn on device causes  
5 the frames encoded with the on-screen display to be supplied  
6 to a digital television in response to the first I frame  
7 marker, and wherein the on-screen display turn on device  
8 causes original frames to be supplied to the digital  
9 television in response to the second I frame marker.

10           19. The MPEG on-screen display coder of claim 18  
11 wherein the MPEG encoder signals the first and second I  
12 frame markers when corresponding original I frames are  
13 received.

14           20. The MPEG on-screen display coder of claim 1  
15 wherein the MPEG encoder is arranged to generate an I frame  
16 having a solid color background and an on-screen display,  
17 and wherein the MPEG encoder generates a P frame predicted  
18 from the I frame with residuals and motion vectors set equal  
19 to zero.

1           21. The MPEG on-screen display coder of claim 1  
2 wherein the MPEG encoder is arranged to encode frames with  
3 the on-screen display by prediction with non-zero motion  
4 vectors in order to encode animated graphics.

1           22. The MPEG on-screen display coder of claim 1  
2 wherein the MPEG encoder is arranged to pass a first I frame  
3 without modification, to predict subsequent P frames based  
4 upon the first I frame, to overlay the on-screen display on  
5 a second I frame, and to predict subsequent P frames based  
6 upon the second I frame.

1           23. The MPEG on-screen display coder of claim 1  
2 wherein the MPEG encoder is arranged to encode frames by  
3 mixing original video in a window of reduced size with the  
4 on-screen display.

1           24. The MPEG on-screen display coder of claim 1  
2 wherein the MPEG encoder is arranged to pass unchanged I  
3 frames.

1           25. The MPEG on-screen display coder of claim 24  
2 wherein the MPEG encoder is arranged to encode a first P  
3 frame by predicting the first P frame from a preceding I  
4 frame with residuals in the predicted first P frame  
5 containing the on-screen display and with motion vectors set  
6 equal to zero, and wherein the MPEG encoder is arranged to  
7 encode subsequent P frames based upon the predicted first P  
8 frame with residuals and motion vectors set equal to zero.

1  
2  
3  
4  
5  
6  
7  
8  
9           26. The MPEG on-screen display coder of claim 25  
wherein the MPEG encoder is arranged to supply first and  
second I frame markers to the on-screen display turn on  
device, wherein the on-screen display turn on device causes  
the frames encoded with the on-screen display to be supplied  
to a digital television in response to the first I frame  
marker, and wherein the on-screen display turn on device  
causes original frames to be supplied to the digital  
television in response to the second I frame marker.

1           27. The MPEG on-screen display coder of claim 26  
2 wherein the MPEG encoder signals the first and second I  
3 frame markers when corresponding original I frames are  
4 received.



1           28. The MPEG on-screen display coder of claim 1  
2 wherein the MPEG encoder is arranged to encode I frames with  
3 the on-screen display.

1           29. The MPEG on-screen display coder of claim 28  
2 wherein the MPEG encoder is arranged to encode subsequent P  
3 frames by prediction based upon the encoded I frames with  
4 residuals and motion vectors set equal to zero.

1           30. The MPEG on-screen display coder of claim 29  
2 wherein the MPEG encoder is arranged to supply first and  
3 second I frame markers to the on-screen display turn on  
4 device, wherein the on-screen display turn on device causes  
5 the frames encoded with the on-screen display to be supplied  
6 to a digital television in response to the first I frame  
7 marker, and wherein the on-screen display turn on device  
8 causes original frames to be supplied to the digital  
9 television in response to the second I frame marker.

1           31. The MPEG on-screen display coder of claim 30  
2 wherein the MPEG encoder signals the first and second I  
3 frame markers when corresponding original I frames are  
4 received.

1                   32. An MPEG on-screen display coder comprising:  
2                   an MPEG encoder arranged to encode frames of a  
3                   selected program with an on-screen display; and,  
4                   a multiplexer arranged to replace original frames  
5                   with the encoded frames for supply to a digital television  
6                   receiver.

1                   33. The MPEG on-screen display coder of claim 32  
2                   wherein the encoded frames have a time base which is  
3                   independent of the original frames.

1                   34. The MPEG on-screen display coder of claim 33  
2                   wherein the on-screen display is overlaid on a solid color  
3                   background.

1                   35. The MPEG on-screen display coder of claim 33  
2                   wherein the MPEG encoder is arranged to calculate a video  
3                   hold off time dependent upon a number of frames in a decoder  
4                   buffer of the digital television receiver and to use the  
5                   video hold off time so as to prevent overflow of the decoder  
6                   buffer.

1           36. The MPEG on-screen display coder of claim 35  
2 wherein the MPEG encoder controls the multiplexer with the  
3 video hold off time so as to permit the encoded frames to be  
4 supplied to the digital television receiver when the video  
5 hold off time expires.

1           37. The MPEG on-screen display coder of claim 32  
2 wherein the encoded frames have a time base which is slaved  
3 to the original frames.

1           38. The MPEG on-screen display coder of claim 37  
2 wherein the on-screen display is overlaid on a solid color  
3 background.

1           39. The MPEG on-screen display coder of claim 37  
2 wherein the MPEG encoder is arranged to supply I frame  
3 markers, and wherein the multiplexer is controlled in  
4 response to the I frame markers so as to begin supplying  
5 encoded frames to the digital television receiver with one I  
6 frame and to resume supplying the original frames to the  
7 digital television receiver with another I frame.

1           40. The MPEG on-screen display coder of claim 37  
2 wherein the MPEG encoder is arranged to supply a video I  
3 frame marker and an on-screen display I frame marker,  
4 wherein the multiplexer is controlled in response to the on-  
5 screen display I frame marker so as to begin supplying  
6 encoded frames to the digital television receiver with one I  
7 frame, and wherein the multiplexer is controlled in response  
8 to the video I frame marker so as to resume supplying the  
9 original frames to the digital television receiver with  
10 another I frame.

11           41. The MPEG on-screen display coder of claim 40  
12 wherein the MPEG encoder supplies the on-screen display I  
13 frame marker when the MPEG encoder generates an encoded I  
14 frame, and wherein the MPEG encoder signals the video I  
15 frame marker when an original I frame is received.

1           42. The MPEG on-screen display coder of claim 32  
2 wherein the on-screen display is overlaid on video.

1           43. The MPEG on-screen display coder of claim 42  
2 wherein the MPEG encoder is arranged to pass unchanged I  
3 frames.

1           44. The MPEG on-screen display coder of claim 43  
2 wherein the MPEG encoder is arranged to encode a first P  
3 frame by predicting the first P frame from a preceding I  
4 frame with residuals in the predicted first P frame  
5 containing the on-screen display and with motion vectors set  
6 equal to zero, and wherein the MPEG encoder is arranged to  
7 encode subsequent P frames based upon the predicted first P  
8 frame with residuals and motion vectors set equal to zero.

1           45. The MPEG on-screen display coder of claim 44  
2 wherein the MPEG encoder is arranged to supply first and  
3 second I frame markers, wherein the multiplexer is  
4 controlled in response to the first I frame marker so as to  
5 begin supplying encoded frames to the digital television  
6 receiver with one I frame, and wherein the multiplexer is  
7 controlled in response to the second I frame marker so as to  
8 resume supplying the original frames to the digital  
9 television receiver with another I frame.

1           46. The MPEG on-screen display coder of claim 42  
2 wherein the MPEG encoder is arranged to encode I frames with  
3 the on-screen display.

1           47. The MPEG on-screen display coder of claim 46  
2 wherein the MPEG encoder is arranged to encode subsequent P  
3 frames by prediction based upon the encoded I frames with  
4 residuals and motion vectors set equal to zero.

1           48. The MPEG on-screen display coder of claim 47  
2 wherein the MPEG encoder is arranged to supply first and  
3 second I frame markers, wherein the multiplexer is  
4 controlled in response to the first I frame marker so as to  
5 begin supplying encoded frames to the digital television  
6 receiver with one I frame, and wherein the multiplexer is  
7 controlled in response to the second I frame marker so as to  
8 resume supplying the original frames to the digital  
9 television receiver with another I frame.

1           49. The MPEG on-screen display coder of claim 32  
2 wherein the MPEG encoder is arranged to generate an I frame  
3 having a solid color background and an on-screen display,  
4 and wherein the MPEG encoder generates a P frame predicted  
5 from the I frame with residuals set equal to zero.

1           50. The MPEG on-screen display coder of claim 32  
2 wherein the MPEG encoder is arranged to encode frames with  
3 the on-screen display by prediction with non-zero motion  
4 vectors in order to encode animated graphics.

1           51. The MPEG on-screen display coder of claim 32  
2 wherein the MPEG encoder is arranged to pass a first I frame  
3 without modification, to predict subsequent P frames based  
4 upon the first I frame, to overlay the on-screen display on  
5 a second I frame, and to predict subsequent P frames based  
6 upon the second I frame.

1           52. The MPEG on-screen display coder of claim 32  
2 wherein the MPEG encoder is arranged to encode frames by  
3 mixing original video in a window of reduced size with the  
4 on-screen display.

1           53. The MPEG on-screen display coder of claim 32  
2 wherein the MPEG encoder is arranged to pass unchanged I  
3 frames.

1           54. The MPEG on-screen display coder of claim 53  
2 wherein the MPEG encoder is arranged to encode a first P  
3 frame by predicting the first P frame from a preceding I  
4 frame with residuals in the predicted first P frame  
5 containing the on-screen display and with motion vectors set  
6 equal to zero, and wherein the MPEG encoder is arranged to  
7 encode subsequent P frames based upon the predicted first P  
8 frame with residuals and motion vectors set equal to zero.

1           55. The MPEG on-screen display coder of claim 54  
2 wherein the MPEG encoder is arranged to supply first and  
3 second I frame markers, wherein the multiplexer is  
4 controlled in response to the first I frame marker so as to  
5 begin supplying encoded frames to the digital television  
6 receiver with one I frame, and wherein the multiplexer is  
7 controlled in response to the second I frame marker so as to  
8 resume supplying the original frames to the digital  
9 television receiver with another I frame.

1           56. The MPEG on-screen display coder of claim 32  
2 wherein the MPEG encoder is arranged to encode I frames with  
3 the on-screen display.



1           57. The MPEG on-screen display coder of claim 56  
2 wherein the MPEG encoder is arranged to encode subsequent P  
3 frames by prediction based upon the encoded I frames with  
4 residuals and motion vectors set equal to zero.

1           58. The MPEG on-screen display coder of claim 57  
2 wherein the MPEG encoder is arranged to supply first and  
3 second I frame markers, wherein the multiplexer is  
4 controlled in response to the first I frame marker so as to  
5 begin supplying encoded frames to the digital television  
6 receiver with one I frame, and wherein the multiplexer is  
7 controlled in response to the second I frame marker so as to  
8 resume supplying the original frames to the digital  
9 television receiver with another I frame.

1           59. The MPEG on-screen display coder of claim 32  
2 wherein the multiplexer is arranged to add make-up packets  
3 to each encoded frame as necessary to ensure that each  
4 encoded frame has as many transport packets as the original  
5 frames.

1           60. The MPEG on-screen display coder of claim 59  
2 wherein the make-up packets are null packets.

1           61. The MPEG on-screen display coder of claim 59  
2 wherein the make-up packets are Program Map Table packets.

1           62. An MPEG on-screen display coder comprising:  
2 a buffer arranged to receive and buffer an MPEG  
3 transport data stream containing frames of a selected  
4 program and frames of a non-selected program;

5 an MPEG encoder arranged to encode frames of the  
6 selected program with an on-screen display; and,

7 a multiplexer arranged to selectively pass to a  
8 digital television receiver the frames of the non-selected  
9 program, the encoded frames of the selected program, and  
10 original frames of the selected program.

11           63. The MPEG on-screen display coder of claim 62  
12 wherein the encoded frames have a time base which is  
13 independent of the original frames of the selected program.

1           64. The MPEG on-screen display coder of claim 62  
2 wherein the encoded frames have a time base which is slaved  
3 to the original frames of the selected program.

1           65. The MPEG on-screen display coder of claim 62  
2 wherein the MPEG encoder is arranged to calculate a video  
3 hold off time dependent upon a number of frames in a decoder  
4 buffer of the digital television receiver and to use the  
5 video hold off time so as to prevent overflow of the decoder  
6 buffer.

1           66. The MPEG on-screen display coder of claim 62  
2 wherein the MPEG encoder is arranged to supply I frame  
3 markers, and wherein the multiplexer is controlled in  
4 response to the I frame markers so as to begin supplying  
5 encoded frames to the digital television receiver with one I  
6 frame and to resume supplying the original frames of the  
7 selected program to the digital television receiver with  
8 another I frame.

1           67. The MPEG on-screen display coder of claim 62  
2 wherein the MPEG encoder is arranged to supply a video I  
3 frame marker and an on-screen display I frame marker,  
4 wherein the multiplexer is controlled in response to the on-  
5 screen display I frame marker so as to begin supplying  
6 encoded frames to the digital television receiver with one I  
7 frame, and wherein the multiplexer is controlled in response  
8 to the video I frame marker so as to resume supplying the

9 original frames of the selected program to the digital  
10 television receiver with another I frame.

1 68. The MPEG on-screen display coder of claim 67  
2 wherein the MPEG encoder supplies the on-screen display I  
3 frame marker when the MPEG encoder generates an encoded I  
4 frame, and wherein the MPEG encoder signals the video I  
5 frame marker when an original I frame of the selected  
6 program is received.

69. The MPEG on-screen display coder of claim 62  
wherein the on-screen display is overlaid on a solid color  
background.

70. The MPEG on-screen display coder of claim 62  
wherein the on-screen display is overlaid on video.

1 71. The MPEG on-screen display coder of claim 62  
2 wherein the MPEG encoder is arranged to pass unchanged I  
3 frames.

1           72. The MPEG on-screen display coder of claim 71  
2 wherein the MPEG encoder is arranged to encode a first P  
3 frame by predicting the first P frame from a preceding I  
4 frame with residuals in the predicted first P frame  
5 containing the on-screen display and with motion vectors set  
6 equal to zero, and wherein the MPEG encoder is arranged to  
7 encode subsequent P frames based upon the predicted first P  
8 frame with residuals and motion vectors set equal to zero.

1           73. The MPEG on-screen display coder of claim 72  
2 wherein the MPEG encoder is arranged to supply first and  
3 second I frame markers, wherein the multiplexer is  
4 controlled in response to the first I frame marker so as to  
5 begin supplying the encoded frames to the digital television  
6 receiver with one I frame, and wherein the multiplexer is  
7 controlled in response to the second I frame marker so as to  
8 resume supplying the original frames of the selected program  
9 to the digital television receiver with another I frame.

1           74. The MPEG on-screen display coder of claim 62  
2 wherein the MPEG encoder is arranged to encode I frames with  
3 the on-screen display.

1           75. The MPEG on-screen display coder of claim 74  
2 wherein the MPEG encoder is arranged to encode subsequent P  
3 frames by prediction based upon the encoded I frames with  
4 residuals and motion vectors set equal to zero.

1           76. The MPEG on-screen display coder of claim 75  
2 wherein the MPEG encoder is arranged to supply first and  
3 second I frame markers, wherein the multiplexer is  
4 controlled in response to the first I frame marker so as to  
5 begin supplying the encoded frames to the digital television  
6 receiver with one I frame, and wherein the multiplexer is  
7 controlled in response to the second I frame marker so as to  
8 resume supplying the original frames of the selected program  
9 to the digital television receiver with another I frame.

1           77. The MPEG on-screen display coder of claim 62  
2 wherein the MPEG encoder is arranged to generate an I frame  
3 having a solid color background and an on-screen display,  
4 and wherein the MPEG encoder generates a P frame predicted  
5 from the I frame with zero residual.

1           78. The MPEG on-screen display coder of claim 62  
2 wherein the MPEG encoder is arranged to encode frames with  
3 the on-screen display by prediction with non-zero motion  
4 vectors in order to encode animated graphics.

1           79. The MPEG on-screen display coder of claim 62  
2 wherein the MPEG encoder is arranged to pass a first I frame  
3 without modification, to predict subsequent P frames based  
4 upon the first I frame, to overlay the on-screen display on  
a second I frame, and to predict subsequent P frames based  
upon the second I frame.

1           80. The MPEG on-screen display coder of claim 62  
2 wherein the MPEG encoder is arranged to encode frames by  
3 mixing original video of the selected program in a window of  
4 reduced size with the on-screen display.

1           81. The MPEG on-screen display coder of claim 62  
2 wherein the multiplexer is arranged to add make-up packets  
3 to each encoded frame as necessary to ensure that each  
4 encoded frame has as many transport packets as an original  
5 frame of the selected program.

1                   82. The MPEG on-screen display coder of claim 81  
2 wherein the make-up packets are null packets.

1                   83. The MPEG on-screen display coder of claim 81  
2 wherein the make-up packets are Program Map Table packets.

0533069-061199  
657790-6908860